Advantages of PLL Circuitry in Altera Devices

TECHNICAL BRIEF 10 JULY 1996

Altera is offering two new features for high-density PLDs—called ClockLock and ClockBoost—that use a phase-locked loop (PLL). The ClockLock feature minimizes on-chip clock skew, significantly increasing performance. The ClockBoost feature increases clock frequencies by as much as four times the incoming clock rate, improving system bandwidth. Together, these enhancements provide significant breakthroughs in system performance and bandwidth. See Figures 1 and 2.

Figure 1. ClockLock Circuitry

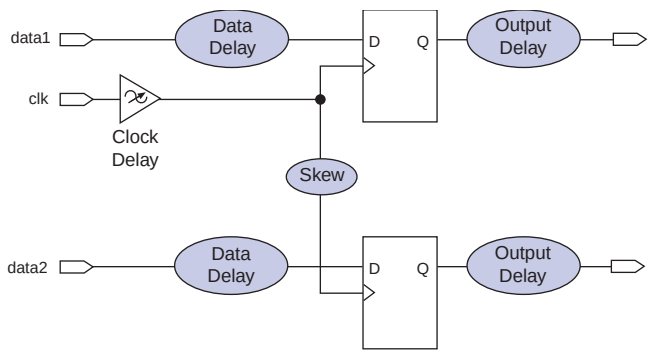
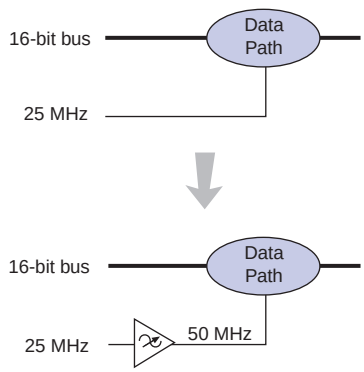


Figure 2. ClockBoost Circuitry



The revolutionary ClockLock and ClockBoost features greatly reduce clock delay, clock skew, and data delay within a device as shown in the following equations. Since larger devices tend to have longer delays and greater skew, PLL circuitry is especially important for high-density devices, such as the EPF10K100, the largest member of the FLEX 10K family. The benefits to customers are increased PLD performance and utilization.

$$t_{CO} = \text{clock delay}_{\mathbf{0}} + \text{clock skew}_{\mathbf{0}} + \text{register delay} + \text{output delay}$$

$$t_{SU} = \text{register set-up} + \text{data delay} - \text{clock delay}_{\mathbf{0}}$$

ClockLock: Faster System Performance

The ClockLock feature uses the PLL to minimize on-chip clock skew, significantly improving performance. For example, by using the ClockLock circuitry in FLEX 10K devices, designers should see a worse case t_{SU} and t_{CO} of 6 ns and 3.6 ns, respectively, which would increase the expected system performance by more than 60%. This type of performance increase will help designers meet the high-speed bus interface requirements of the future. See Table 1.

Table 1. EPF10K100-3 Timing Comparison

Timing Parameter	Without ClockLock (Preliminary)	With ClockLock (Preliminary)
t_{CO}	11.5 ns	8.5 ns
t_{SU}	7.0 ns	3.6 ns
f_{SYS}	54 MHz	83 MHz

ClockBoost: Increased System Bandwidth & Reduced Area

The ClockBoost feature uses the PLL for clock multiplication, significantly reducing the logic resources required to implement functions. This reduction in gate requirements is achieved through a technique called time-domain multiplexing. For example, a design that requires a 32-bit data path function running at 40 MHz can be implemented with a 16-bit data path function running internally at 80 MHz, achieving the same functionality with half the logic resources and I/O requirements. See Table 2.

Table 2. Reduced Logic Resource Requirements Achieved via ClockBoost in the EPF10K100

Circuit	Without ClockBoost (LEs)	With ClockBoost (LEs)
8 x 8 Multiplier	330	198

In cases where time-domain multiplexing is not needed, designers can use a slower external system clock, and internally multiply it for use within the Altera PLD. The advantage in a slower system clock is simpler PCB design, as there would be less ringing on the clock traces.

Altera: The PLL Leader

Altera is the only PLD vendor that offers devices with a PLL, as shown in Table 3. The ClockLock and ClockBoost features will be available in the Altera FLEX 10K and MAX 7000S families of high-density programmable logic devices.

Table 3. PLD Families Offering PLL Circuitry

Device Density (Gates)	Altera	AMD	Lattice	Lucent	Xilinx
0 – 25,000	MAX 7000S FLEX 10K	—	—	—	—
25,000 – 50,000	FLEX 10K	—	—	—	—
50,000 – 100,000	FLEX 10K	—	—	—	—

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